SHRIHARI

ABOUT ME

Driven by my zeal for innovation and technology, I am an upcoming VLSI Design Engineer and an open-source enthusiast emphasizing freedom to chip design. I look forward to create a valid imprint on innovation, trying to address unsolved engineering challenges

CONTACT

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ACADEMIC INTERESTS

- RTL and Logic Design
- Computer Architecture
- VLSI Physical Design
- Internet of Things
- Embedded System Design
- Electronic Design Automation

PROFESSIONAL MEMBERSHIPS

- RISC-V International
- Linux Foundation
- Institution of Electronics and Telecommunication Engineers (IETE)
- OSFPGA

LANGUAGES

- Tamil - *Native Proficiency*
- English - *Full Professional Proficiency*
- French - *Limited Working Proficiency*

EDUCATION

PSG College of Technology

Bachelor of Engineering - Electronics and Communications
July 2018 - May 2022 (Expected graduation)

- GPA 9.92/10, Best Outgoing Student of 2018-2022
- Department Topper, Semesters 1-6
- Secretary, Astronomy Club

Lisieux Matriculation and Higher Secondary School

High School
Graduated May 2018

- School rank 2 - Grade 12 - HSC Examination
- School rank 1 - Grade 10 - SSLC Examination
- Teaching Assistant for Grade 10, Mathematics

EXPERIENCE

Design Engineer - Intern

Silicon Labs | January 2022 - Present

- Verification of Sub-Systems in Wireless SoCs
- Develop additional features for internal EDA Tools and interfacing with commercial tools

Open Source Developer

Redwood EDA | October 2021 - Present

- Develop IP Design and remote FPGA frameworks based on TL-Verilog to enrich its ecosystem
- Build TL-Verilog based Hardware Accelerator Kernel Prototyping flow for Xilinx FPGAs

RTL Design Engineer - Intern

InCore Semiconductors Pvt Ltd | July 2021 - January 2022

- Carry out micro-architectural optimizations on RISC-V Processors
- Develop accelerator/co=processor interconnects for In-house RISC-V processors

Teaching Assistant

VLSI System Design Pvt. Ltd

- Developed Remote FPGA Lab infrastructure
- Assisted in the course "FPGA - Fabric, Design and Architecture"
- Developed and prototyped RISC-V Cores on custom FPGA Fabrics

Founder - Technowiz Academy

September 2018 - present | technowiz.org

- Offer tie-ups to High schools in the state for Robotics and Basic Electronics Workshops
- Organize sessions and deliver technical talks for workshops
- Develop and maintain business plans and finances

PUBLICATIONS

"RISC-V ISA based Autonomous Quad-Plane using Shakti C-64 Vajra Processor", International Journal of Scientific and Engineering Research, Vol 12, Issue 3, March 2021.

"Cost Effective IoT Enabled Automation of Spray Pyrolizer", International Research Journal of Engineering and Technology, Vol.8, Issue 3, March 2021.

SKILLS

Programming and Scripting

- Python
- RISC-V Assembly
- C
- C++
- Bourne Shell Scripting

HDL & HL-HDL

- Verilog HDL
- System Verilog
- TL-Verilog
- Bluespec System Verilog

Version Control

- Git and Github

Software Tools

VLSI Front-end

- Vivado Design Suite
- Yosys (Synthesis)
- Questasim

VLSI Back-end

- Cadence Virtuso
- Mentor Graphics - Tanner EDA
- OpenLANE (RTL to GDSII)
- Qflow (RTL to GDSII)
- Magic (Layout)

SPICE Tools

- ngspice
- Multisim

PCB Design

- Altium Designer
- Autodesk Eagle

Others

- MATLAB and Simulink
- Keil uVision
- Autodesk Fusion360
- Wordpress (Web development)

Hardware Tools

- Digital Storage Oscilloscope
- Mixed Signal Oscilloscope
- FPGA: Zynq, Artix, Cyclone-V
- Arduino UNO, MEGA 2560
- Raspberry Pi 4
- Tiva Launchpad
- Nordic Thingy
- NodeMCU
- 3-D Printers

UNDERGRADUATE COURSE WORK

Electronics

- Digital Electronics
- Computer Architecture
- Digital System Design using Verilog HDL
- VLSI Design
- Low Power VLSI Design
- Embedded Systems Design
- Microprocessors and Microcontrollers
- Circuit Theory
- Electron Devices
- Analog Electronics

Communication Systems

- Analog Communication
- Digital Communication
- Information Theory
- Electromagnetic Field Theory
- Transmission Lines and Antennas
- Signals and Systems
- Digital Signal Processing

"Queue based Algorithmic Solution and Hardware Realization of Autonomous Multi Level Car Parking System" in Industrial Automation and Robotics Research. Lambert Academic Publishing, August 2021, ch 4, pp 45-61.

FUNDED PROJECTS

COST EFFECTIVE IOT ENABLED AUTOMATION OF SPRAY PYROLIZER

Thin Film Center of Excellence, PSG College of Technology

- IoT enabled design and development of a Spray pyrolizer to fabricate Thin-Films
- Prototype aimed at promoting remote collaborative research with automated measurement and analytics
- Funded by PSG Science and Technology Entrepreneurial Park

ACADEMIC PROJECTS

Development of Co-Processor Interconnect for RISC-V CPU Cores

A instruction agnostic hardware accelerator adapter for an in-house RISC-V Processor was designed based on the Core-V X-If specification and implemented in Bluespec System Verilog. This provides a unified framework for RISC-V CPU Cores to Implement ISA extensions or interface hardware accelerators and share the accelerator and co-processors among multiple cores.

RPHAX - Rapid Prototyping of Hardware Accelerators on Xilinx FPGAs

RPHAX provides a quick automation flow to develop and prototype hardware accelerators on Xilinx FPGAs using TL-Verilog/Verilog/SystemVerilog. It automates IP Packaging with standard ARM AMBA Interfaces and user definable custom interfaces, creating block design and bitstream generation, enabling users to quickly test hardware accelerators and develop software in PYNQ or Vitis

Physical Design of PicoRV32 using OpenLANE with SKY130 PDK

A complete RTL to GDSII flow was executed for PicoRV32 with custom designed and characterised standard cells in addition to Skywater's cells with SKY130PDK using OpenLANE. A clock speed of 100Mhz was achieved. DRC and LVS were successful.

Transaction Level design of an RV32IC RISC-V Core and Physical Design with 130nm PDK

A RV32IC based in-order 5 stage pipelined RISC-V core was developed at the transaction level using the new TL-Verilog. System Verilog code was generated and synthesized using Skywater130 PDK. A complete RTL to GDSII flow was carried out with Openlane and SKY130 PDK

Development of RISC-V ISA based Flight Controller using Shakti Microprocessor

The control system was designed for a multirotor in SIMULINK and the Embedded C-code for RISC-V ISA was developed. The functionality is verified by using Shakti C-64 Vajra Processor realized on Xilinx Artix-7 35T FPGA. The objective is to develop a multipurpose flight controller using Shakti Microprocessor as a part of “Swadeshi Microprocessor Challenge 2020”, by Government of India(Quarter-Finalist). This project was selected fpr CISCO's "thinqubator 2020" incubation program

SIHA - Smart Intelligent Home Assistant

A complete Home automation system was developed and deployed using Home Assistant Server and NodeRed. Devices are automated with custom PCBs powered by ESP8266 and ML-based Security system from “Hikvision” Platform using Onvif and DeepStack. Alexa support was also integrated. This project was selected for CISCO's "thinqubator 2020" incubation program

Computer Science

- Operating Systems
- Relational Database Management Systems
- Data Structures and Algorithms
- Programming in C

Engineering Mathematics

- Advanced Calculus
- Complex Variables and Transforms
- Linear Algebra and Numerical Analysis
- Probability and Random Processes

ONLINE COURSES

- *Computer Architecture Winter School, National Supercomputing Mission, Government of India. (Selected out of 1000+ applicants in India)*
- *Building a RISC-V CPU Core, Linux Foundation*
- *Advanced Physical design with OpenLane using SKY130 PDK, VLSI System Design Corporation.*
- *Python Specialisation, University of Michigan*
- *Design thinking for innovation, University of Virginia*
- *Enterprise Design Thinking, IBM*
- *Team Essentials for AI, IBM*
- *Android Enterprise Associate, Google*
- *Blockchain and Ethereum, EMURGO Academy*
- *Object Localisation using Tensorflow, Coursera*
- *Build a full website with WordPress, Rhyme*
- *"Cybersecurity Practices for Industrial Control Systems" from US Department of Homeland and Security*
- *"Introduction to Blockchain and Bitcoin", by EMURGO Academy, Japan*
- *"Ethereum Development", by EMURGO Academy*
- *HTML Fundamentals" from Sololearn*
- *"JavaScript Tutorials" from Sololearn*

RTL Design and Synthesis of Sequential binary Multiplier using SKYWATER130 PDK

An RTL design of Sequential Binary Multiplier was designed using Verilog HDL, verified and Synthesized with Skywater130nm PDK

ESP8266 based Wi-Fi De-authentication attack

The de-authentication attack was performed exploiting the flaw in IEEE 802.11 Standard which was used to send a de-authentication frame at any time, with a spoofed source address resulting in periodic de-authentication of the network rendering it unusable by the clients. This can be prevented with IEEE 802.11w standard with protected management frames (PMF) enabled in both the client and the access point.

Modified SIR model of COVID-19 based on Exponential Growth Projection

A modified Stochastic SIR model for estimating an epidemic curve early in an outbreak by projecting an exponential growth to select the initial conditions is developed

ACHIEVEMENTS

Founder - Technowiz

- Selected for CISCO THINQUBATOR 2021
- Organized workshops and delivered technical talks to students at Lisieux Matriculation and Higher Secondary School

Undergraduate School

- Semi-Finalist in Terasic's InnovateFPGA 2021 sponsored by Intel Quarter-Finalist in "Swadeshi Microprocessor Challenge 2020" conducted by the Government of India
- Department Topper in Semester 1 to 6
- Secured First place in "Cryptera 2021", a paper presentation contest by CIT, Coimbatore.
- Secured First place in "Process it", a MATLAB Coding Competition at YUGAM 2020, Kumaraguru College of Technology.
- Secured First place in "Splash your Antenna", an Antenna design contest at YUGAM 2020, Kumaraguru College of Technology.
- Won First Place in IoT Hackathon conducted at SAARANG 2k18, IIT Madras.
- Won Second prize in Mathematics Talent Search Contest conducted by Ramanujan Association of Mathematics, PSG College of Technology
- Won First prize in SPECTRE in HERTZ 2k18 conducted by ECEA, PSG College of Technology
- Won Third Prize in ELECTROCURIEUX in HERTZ 2k18 conducted by ECEA, PSG College of Technology
- Won First Prize in PHYSINNORATIO conducted by SIR CV Raman Physics Association, PSG College of Technology for the paper titled "Cost Effective IoT enabled automation of Spray Pyrolizer"

High School

- Secured International Rank 215 at International Mathematics Olympiad conducted by SOF in 2018.
- Secured School Second in HSC 2018.
- Awarded the "Best Student OF The Year 2017"
- Secured District Second and School First in SSLC 2016