Shrihari Gokulachandran

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Profile

Driven by my zeal for Silicon design, I have acquired a robust knowledge on ASIC Design and Verification, Hardware accelerators, FPGAs, and CPU Microarchitecture. Additionally, I have a full stack hands-on experience right from the RTL to GDSII through open-source PDKs. I look forward to creating a valid imprint on innovation, trying to address unsolved engineering challenges through my internship starting Summer 2023.

Education

THE UNIVERSITY OF TEXAS AT AUSTIN, Texas, USA *August 2022 – May 2027 (Expected)*

MS and PhD - Electrical and Computer Engineering

- Concentration in Architecture, Computer Systems, and Embedded Systems
- Courses (currently enrolled): Computer Architecture, Verification of Digital Systems, Research Problems

PSG COLLEGE OF TECHNOLOGY, Coimbatore, India *August 2018 – May 2022*

Bachelor of Engineering - Electronics and Communication Engineering, GPA: 9.92/10

- Gold Medalist - Class of 2022, Best Outgoing Student - Class of 2022 and Dr. Jeyaraman Best Project Award
- Related coursework: Computer Organization and Architecture, Embedded Systems, Microprocessors and Microcontrollers, Internet of Things, Digital Electronics, VLSI Design, Digital Signal Processing, Advanced Physical Design using 130nm PDK (VSD), Building a RISC-V CPU (Linux Foundation)

Experience

TEACHING ASSISTANT | THE UNIVERSITY OF TEXAS AT AUSTIN *September 2022 - Present*

- ECE 306 Introduction to Computing, Leading Recitation/Problem solving classes and assisting lectures

OPEN-SOURCE DEVELOPER | GOOGLE SUMMER OF CODE *May 2022 – August 2022*

- Developing "1st CLaaS for PYNQ FPGAs", an automated hardware accelerator integration framework with remote FPGA capabilities
- Integration in Makerchip.com, a cloud-based IDE for TL-Verilog/Verilog to conduct FPGA development within the browser

DESIGN ENGINEER - INTERN | SILICON LABS, India *January 2022 – July 2022*

- Developed frameworks for migration and integration of legacy projects in Silicon Labs Design Environment
- Developed and Integrated Golden Reference Models for QSPI AES modules in Security Sub Systems and rectified critical design bugs in Security Sub-Systems
- Worked on Internal VCs for ARM Low Power Interface, Silicon Labs Peripheral Reflex System, AXI and SPI
- Automated GPIO De-mux testbench generation, resulting in rapid testing for varied test configurations
- Responsible for Formal Verification bring-up in upcoming projects

RTL DESIGN ENGINEER – INTERN | INCORE SEMICONDUCTORS, India *July 2021 – January 2022*

- Architected and developed custom Co-processor interconnects for RISC-V Processors
- Updated SoC generation frameworks with interconnect generation support

TEACHING ASSISTANT | VLSI SYSTEM DESIGN, India *November 2021, June 2022*

- Developed Remote FPGA Lab Infrastructure and assisted in the course "FPGA – Fabric, Design and Architecture"
- Developed Custom FPGAs and Prototyped RISC-V Cores on Xilinx FPGAs and Custom FPGAs

FOUNDER | TECHNOWIZ, India *September 2018 – Present*

- Founded a startup and associated with high schools to offer workshops on Robotics, DIY Electronics and Programming
- Developed makerspaces and organized hackathons

Academic Projects

HARDWARE ACCELERATOR EXTENSION INTERFACE FOR RISC-V CPUS

- Researched open-source co-processor interfaces and developed co-processor agnostic accelerator adapter for a RISC-V Core
- Integrated and implemented the adapter in RTL on a RISC-V Core and a test co-processor

RPHAX - RAPID PROTOTYPING OF HARDWARE ACCELERATORS ON XILINX FPGAS

- Designed and developed automation frameworks for IP Packaging (AXI4-Lite, AXI Stream), Block Design and bitstream generation
- Achieved a "single-command" automation flow to go from Logic Design to Bitstream, accelerating development life cycle of hardware accelerator prototyping on Zynq FPGAs

TRANSACTION LEVEL DESIGN OF MULTISTAGE RISC-V RV32IC CPU CORE AND PHYSICAL DESIGN ON 130NM PDK

- Designed a multi-stage ((1-6) pipelined RISC-V CPU Core using Transaction Level Verilog and simulated by running assembly programs
- Conducted the RTL to GDSII flow with open-source tools and 130nm Skywater PDK. Met timing and obtained a DRC, LVS free GDSII

RTL DESIGN OF MODIFIED AES-256 ACCELERATOR

- Enhanced the randomness in AES by modifying the Byte Substitution and Cipher round algorithm achieving a 1.02% increase in avalanche effect.
- Achieved a 38x speedup on the Zynq based design in encryption and decryption at a clock rate of 50Mhz

IOT ENABLED AUTOMATION OF SPRAY PYROLIZER *(Funded by PSG Science and Technology Entrepreneurial Park)*

- Developed a remotely manageable Spray Pyrolizer for Thin Film fabrication with data acquisition capabilities, automating sample preparation, obtaining analytics on the cloud and data visualization.
- Resulted in researchers saving time on repetitive tasks and fasten experiment time

SHAKTI MICROPROCESSOR BASED FLIGHT CONTROLLER

- Led a team in developing the control system of a multi-rotor in SIMULINK and generated Embedded C Code.
- The design was tested on SIMULINK, and was also emerged as a Quarter Finalist in the Swadeshi Microprocessor Challenge, a Nation-level Hackathon held by Government of India

SIHA – SMART INTELLIGENT HOME ASSISTANT

- Developed a framework and a ESP8266 based controller to enable IoT and security capabilities in non-IoT devices. This project was selected for incubation by CISCO ThingQbator 2020
- Built Linux server running Home Assistant Framework and deployed it my home.

Skills

PROGRAMMING/SCRIPTING: C, Python, bash, RISC-V Assembly

HDL/HVL: Verilog, System Verilog, Bluespec System Verilog, TL-Verilog

VERSION CONTROL: Git, Perforce, Methodics

SOFTWARE TOOLS: Xilinx Vivado, Intel Quartus, QuestaSim, VCS, MATLAB, Simulink, Yosys, Questa Formal Verification tools, Opensource FPGA & ASIC development tools

HARDWARE TOOLS: FPGAs (Xilinx Artix, Zynq, Intel Cyclone), Microcontrollers (Arduino, ESP8266, Raspberry Pi, 8051), MSO, DSO, Vector Analyzers, 3-D Printers

LANGUAGES: English (Bilingual), Tamil (Native/Bilingual), French (Intermediate Proficiency)

Scan to email or view LinkedIn/GitHub/Portfolio

Achievements

- Semi Finalist – Innovate FPGA hackathon sponsored by Intel, Microsoft, and Analog Devices
- Part of Computer Architecture Winter School, National Super Computing Mission, Government of India. Selected among 1000+ applicants in India
- First Place – "Splash your antenna 2021", an Antenna Design contest, KCT, India
- First Place – IoT Hackathon at "Saarang 2018", IIT Madras, India